IN THE CLAIMS

Claims 1-20 (Canceled)

21. (Original) An apparatus, comprising:

a content addressable memory (CAM) array;

a clock circuit coupled to the CAM array; and

a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clock circuit.

22. (Original) The apparatus of claim 21, wherein the programmable delay circuit comprises:

a plurality of the delay elements to generate a plurality of delayed clock signals;

a programmable register to store information indicating a particular delayed clock signal of the plurality of delayed clock signals; and

a multiplexer coupled with the programmable register and the plurality of delay elements to select the particular delayed clock signal based on the information.

23. (Original) The apparatus of claim 22, wherein the programmable delay circuit further comprises a decoder coupled to the programmable register to decode the information stored in the programmable register.

24. (Original) The apparatus of claim 22, wherein each of the plurality of delay elements provides a different time period of delay to the reference clock signal.

25. (Original) The apparatus of claim 21, wherein the clocked circuit comprises a read circuit for reading data from the CAM array.

26. (Original) The apparatus of claim 21, wherein the clocked circuit comprises a register for storing comparand data for comparison with data of the CAM array.

27. (Original) The apparatus of claim 21, wherein the CAM array comprises a plurality of rows of CAM cells each having a corresponding match line for carrying a match signal indicative of whether comparand data matches data of the corresponding row of CAM cells.

28. (Original) The apparatus of claim 27, wherein the clocked circuit comprises an encoder circuit coupled to the match lines and the programmable delay circuit.

29. (Original) The apparatus of claim 28, wherein the clocked circuit comprises match flag logic coupled to the match lines and the programmable delay circuit.

30. (Original) The apparatus of claim 21, further comprising:

a second clocked circuit; and

a second programmable delay circuit.

Claims 31-42 (Canceled)

43. (Original) A method, comprising:

establishing a connection with a register in a content addressable memory (CAM) device; and

programming the register in the content addressable memory (CAM) device with information representing a value of a delay time period for the generation of a delayed clock signal.

44. (Original) The method of claim 43, further comprising:

generating the delayed clock signal based on a reference clock signal using the programmed information; and

outputting data based on the delayed clock signal.

45. (Original) The method of claim 44, further comprising:

programming the register with additional information representing the value of another delay time period; and

generating the delayed clock signal using the additional information.

46. (Original) The method of claim 44, further comprising:

programming a second register with second information representing the value of a second delay time period; and

generating the delayed clock signal using the second information.

47. (Original) The method of claim 46, further comprising programming the second programmed information based on an anticipated frequency of operation for the reference clock signal.

Claims 48-50 (Canceled)

Claims 51- 53 (Canceled)